

PART III.

Advances in High Performance Backplane Design Based on High Speed Properties of ERmetZD and Optimized Signal Conditioning in FR4 and Low Loss Laminate PCB.

Henri Merkelo and Timothy Hochberg, atSpeed Technologies Corporation
www.atSpeed.net

Roland Moedinger, William MacKillop and Jason Roe, The ERNI Group,
www.erni.de

ABSTRACT

Design criteria and performance tradeoffs are examined in this study that is entirely based on measured and validated properties of fr4 and the newly introduced high speed, backplane connector, named ERmetZD (by the ERNI Components Corporation). Measurements are obtained on a classical configuration consisting of two fr4 daughter cards, two backplane (ERmetZD) connectors and an fr4 backplane. All measurements are ported into software (Oculus) by way of TDR/TDT measurements, validated with a high speed data pattern generator and studied in Oculus for distance vs. data rate tradeoffs. Provisions for passive and active (or both) signal conditioning are also made and are examined. The values for optimized equalization components and optimized tap settings for preemphasis are determined in software. Data rates ranging from **1.25 to 12.5 Gb/s** are propagated in reply to: 7 mil, stripline traces ranging from 12" to lengths exceeding 4 ft. It is shown that the combined high speed properties of ERmetZD, FR4 and optimized signal conditioning offer numerous practical options for substantial size, high speed server designs or for ultrahigh speed card configurations. For example, depending on receiver sensitivity and signal template requirements, results for popular data rates of 2.5, 3.125 and 5 Gb/s show that backplanes with overall 2 to 4 ft trace lengths can be implemented practically. For 10 Gb/s, shorter, but still useful, lengths are practical. It is also shown that even such ultrahigh data rates as 12.5 Gb/s are supported on practical trace lengths. This study discusses the additional advantages that can be gained by implementing low loss dielectrics as well as such new technologies as multivalued logic transceivers.



Agilent Technologies



@Speed